VENUS822-BD Low Power GPS/BD Baseband – Flash Version

FEATURES

- Support GPS, Beidou, QZSS, SBAS
- Ultra fast signal acquisition and TTFF speed
- Perform 16 million time-frequency hypothesis testing per second
- Signal detection better than -165dBm
- Reacquisition sensitivity –157dBm
- Open sky hot start 1 second
- Open sky cold start 29 seconds
- Accuracy 2.5m CEP
- Multipath detection and suppression
- Jamming detection and mitigation
- Support 7-day AGPS and 3-day SAEE
- Tracking 15mA @ 3.3V
- 7mm x 7mm QFN56, RoHS compliant

The Venus822-BD is a high-performance GPS/Beidou baseband processor intended for embedded portable applications. It contains all the baseband function required for GPS/Beidou signal acquisition, tracking, and navigation solution. The Venus822-BD is designed to allow easy integration of GPS/Beidou into application systems.

A dedicated massive-correlator signal parameter search engine enables rapid search of all available satellites and acquisition of very weak signals. An advanced track engine allows weak signal tracking and positioning in severe environments such as urban canyons and under deep foliage.

With exceptional signal acquisition speed, it has very low average power consumption for locate on demand type of applications.

A complete low-cost high-performance GPS/Beidou receiver can be built with Venus822-BD, a compatible GPS/Beidou RF front-end, and a small number of external components.

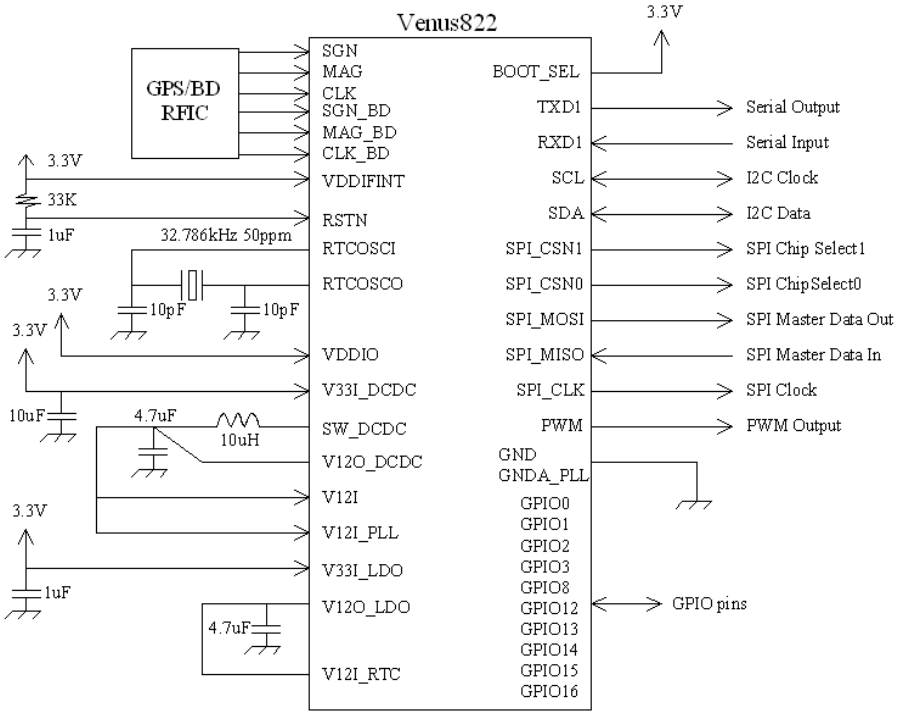


Figure-1 GPS/Beidou Receiver based on Venus822-BD

FUNCTIONAL DESCRIPTION

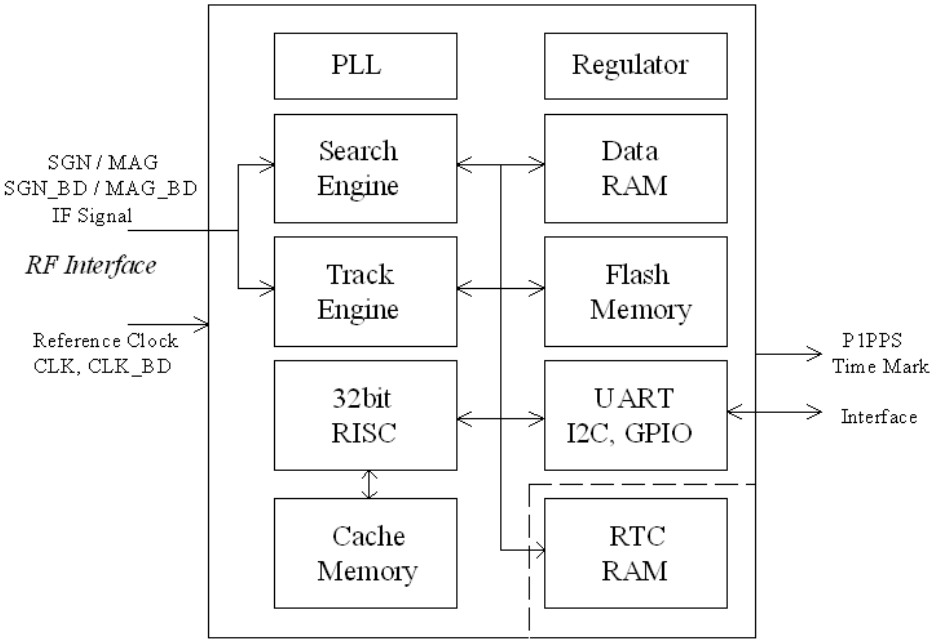


Figure-2 Baseband Processor Functional Diagram

The Venus822-BD implements all the needed function for GPS/Beidou signal acquisition, tracking, decoding, and navigation solution. It is optimized for GPS/Beidou applications requiring high performance. Major blocks within the chip are: GPS/Beidou signal processing engine, 32bit RISC processor, peripheral interface, and memory.

RF Interface

The RF interface supports single-ended IF signal in sign/magnitude format and sampling frequency of 16.367667MHz with +/-0.5ppm accuracy.

GPS/Beidou Signal Processing Engine

The signal-processing engine comprise of a signal parameter search engine and a track engine. Both implement carrier frequency wipe-off, pseudorandom code removal, plus coherent and incoherent integration required for indoors high-sensitivity signal processing.

The signal parameter search engine can be configured to search full code space and several frequencies simultaneously, or full code space of all satellites simultaneously. Massive correlator design allows extremely high signal acquisitions speed and high sensitivity performance.

32bit RISC

The internal 32bit RISC is a 7-stage pipelined processor. The processor handles all time-critical GPS/Beidou related functions, management controls, and navigation solutions.

Cache Memory

Cache memory subsystem consists of 16Kbyte I-cache, and 2Kbyte D-cache.

Battery-Backed RTC and RAM

The real-time clock circuitry and a small block of SRAM is included on-chip to retain time and the necessary GPS/Beidou data for rapid warm start and hot-start operation.

Data RAM

The chip contains SRAM needed for stand-alone operation. The on-chip SRAM is designed for low-power and high-speed single cycle access.

Program ROM

The chip implements program ROM on-chip.

UART

2 sets of UART is supported for Venus822-BD in QFN56 package.

I2C

1 set of I2C is supported for Venus822-BD in QFN56 package.

SPI

SPI with 2 chip-select is supported for Venus822-BD in QFN56 package.

Regulator

3.3V to 1.2V LDO regulator and 3.3V to 1.2V DC/DC switching regulator is implemented on-chip for powering the RTC & Backup SRAM region (V12I_RTC) and the core logic (V12I).

PLL

The signal parameter search engine requires a high frequency clock. It is generated from the GPS reference clock through the on-chip PLL. A divided-down PLL clock is selected to clock the 32bit RISC.

POWER SUPPLIES

The system is partitioned into the following power supply domains:

VDDIO: Digital supply voltage for the I/O interface, supporting 3.3V I/O, 2.97V ~ 3.63V.

V12I: 1.08V ~ 1.32V, the main digital supply voltage for the core logic. It is typically derived from the on-chip 1.2V DC/DC switching regulator or can be provided from an external supply source.

V12I_PLL: 1.08V ~ 1.32V, the analog supply voltage for the internal PLL.

V12I_RTC: 1.08V ~ 1.32V, the digital supply voltage for the battery backed-up RTC and SRAM. Current consumption ~7uA when main chip is inactive, ~1mA when main chip is active.

VDDIFINT: Digital supply voltage for RFIC interface pins (CLK / SGN / MAG), supporting 3.3V I/O or 1.8V I/O. 2.97V ~ 3.63V for 3.3V I/O. 1.62V ~ 1.98V for 1.8V I/O.

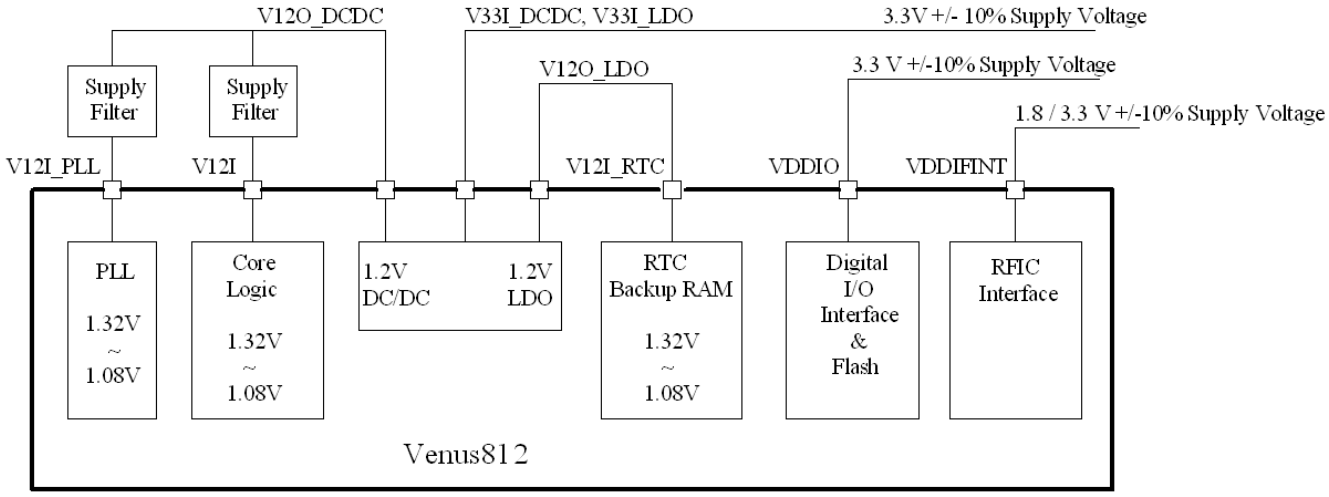


Figure-3 System Power

PIN CONFIGURATION

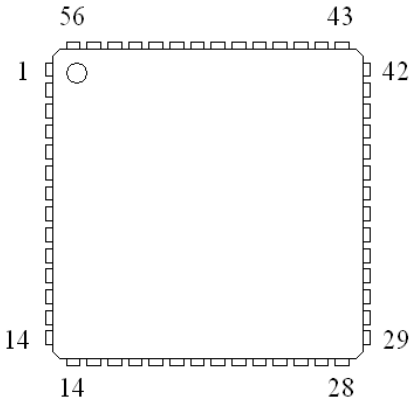


Figure-4 Pin-Out QFN56 (Top-View)

Table-1 Venus822-BD Pin-Out

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	MAG_BD	15	V12I_RTC	29	SPI_MOSI	43	GPIO6
2	SGN_BD	16	V12I_RTC	30	V12I	44	VDDIO
3	GNDA_PLL	17	V12I	31	SPI_CSN0	45	XOUT
4	V12I_PLL	18	RTCOSCI	32	GPIO8	46	XIN
5	V12I_PLL	19	RTCOSCO	33	SPI_CSN1	47	GPIO15
6	V12I	20	V12I_RTC	34	SDA	48	GND
7	VDDIO	21	V12O_DCDC	35	BOOT_SEL	49	GND
8	RSTN	22	V33I_DCDC	36	VDDIO	50	GND
9	GPIO12	23	SW_DCDC	37	V12I	51	CLK
10	GPIO13	24	GPIO1	38	GPIO0	52	SGN
11	GPIO29	25	GPIO2	39	RXD1	53	MAG
12	SCL	26	GPIO3	40	PWM	54	VDDIFINT
13	V12O_LDO	27	GPIO14	41	TXD1	55	V12I
14	V33I_LDO	28	SPI_MISO	42	GPIO16	56	CLK_BD

SIGNAL DESCRIPTION

Table-2 Venus822-BD Signal Description

Signals	Type	Description
Supply		
VDDIO	Power	I/O supply voltage input, 3.3V
V12I_RTC	Power	1.2V backup voltage input
V12I_PLL	Power	1.2V PLL voltage input
V33I_LDO	Power	3.3V supply input to the 1.2V LDO regulator Voltage input range 2.5V ~ 3.6V, DC current ~30uA
V12O_LDO	Power	Regulated output of the 1.2V LDO regulator, max current 24mA. Must not use it to drive baseband core V12I input
V33I_DCDC	Power	3.3V supply input to the 1.2V switching regulator Voltage input range 3.0V ~ 3.6V
V12O_DCDC	Power	Regulated output of the 1.2V switching regulator, max current 100mA
SW_DCDC	Power	Switch pin, connect to inductor
V12I	Power	1.2V core voltage supply input
VDDIFINT	Power	I/O supply voltage input for RFIC interface (CLK, SGN, MAG), 1.8V or 3.3V
CPU Interface		
GPIO0	Bidir	General purpose I/O, 3.3V I/O Alternative function position fix status LED indicator
GPIO1	Bidir	General purpose I/O, 3.3V I/O Alternative function is UART RXD2
GPIO2	Bidir	General purpose I/O, 3.3V I/O Alternative function is UART TXD2
GPIO3	Bidir	General purpose I/O, 3.3V I/O Alternative function is P1PPS
GPIO8	Bidir	General purpose I/O, 3.3V I/O
GPIO12	Bidir	General purpose I/O, 3.3V I/O
GPIO13	Bidir	General purpose I/O, 3.3V I/O
GPIO14	Bidir	General purpose I/O, 3.3V I/O
GPIO15	Bidir	General purpose I/O, 3.3V I/O
GPIO16	Bidir	General purpose I/O, 3.3V I/O
RXD1	Input	UART input, 3.3V I/O
TXD1	Output	UART output, 3.3V I/O
SCL	Bidir	General purpose I/O, 3.3V I/O Alternative function is I2C clock
SDA	Bidir	General purpose I/O, 3.3V I/O Alternative function is I2C data
SPI_CSN1	Bidir	General purpose I/O, 3.3V I/O Alternative function is SPI master chip select #1
SPI_CSN0	Bidir	General purpose I/O, 3.3V I/O Alternative function is SPI master chip select #0
SPI_MOSI	Bidir	General purpose I/O, 3.3V I/O Alternative function is SPI master data out
SPI_MISO	Bidir	General purpose I/O, 3.3V I/O Alternative function is SPI master data in
SPI_CLK	Bidir	General purpose I/O, 3.3V I/O Alternative function is SPI master clock
GPS/BD Interface		
CLK	Input	RFIC GPS reference clock input, 1.8V or 3.3V I/O depending on VDDIFINT
SGN	Input	RFIC GPS sign input, 1.8V or 3.3V I/O depending on VDDIFINT
MAG	Input	RFIC GPS magnitude input, 1.8V or 3.3V I/O depending on VDDIFINT
CLK_BD	Input	RFIC BD reference clock input, 1.8V or 3.3V I/O depending on VDDIFINT
SGN_BD	Input	RFIC BD sign input, 1.8V or 3.3V I/O depending on VDDIFINT
MAG_BD	Input	RFIC BDmagnitude input, 1.8V or 3.3V I/O depending on VDDIFINT

RTC Interface		
RTCOSCI	Input	RTC crystal oscillator input
RTCOSCO	Output	RTC crystal oscillator output
Reset		
RSTN	Input	Active low reset Input, 3.3V I/O
Misc		
BOOT_SEL	Input	Tie to VDDIO for Flash mode. Tie to ground or leave NC for ROM mode

EXTERNAL CONNECTION FOR A WORKING SYSTEM

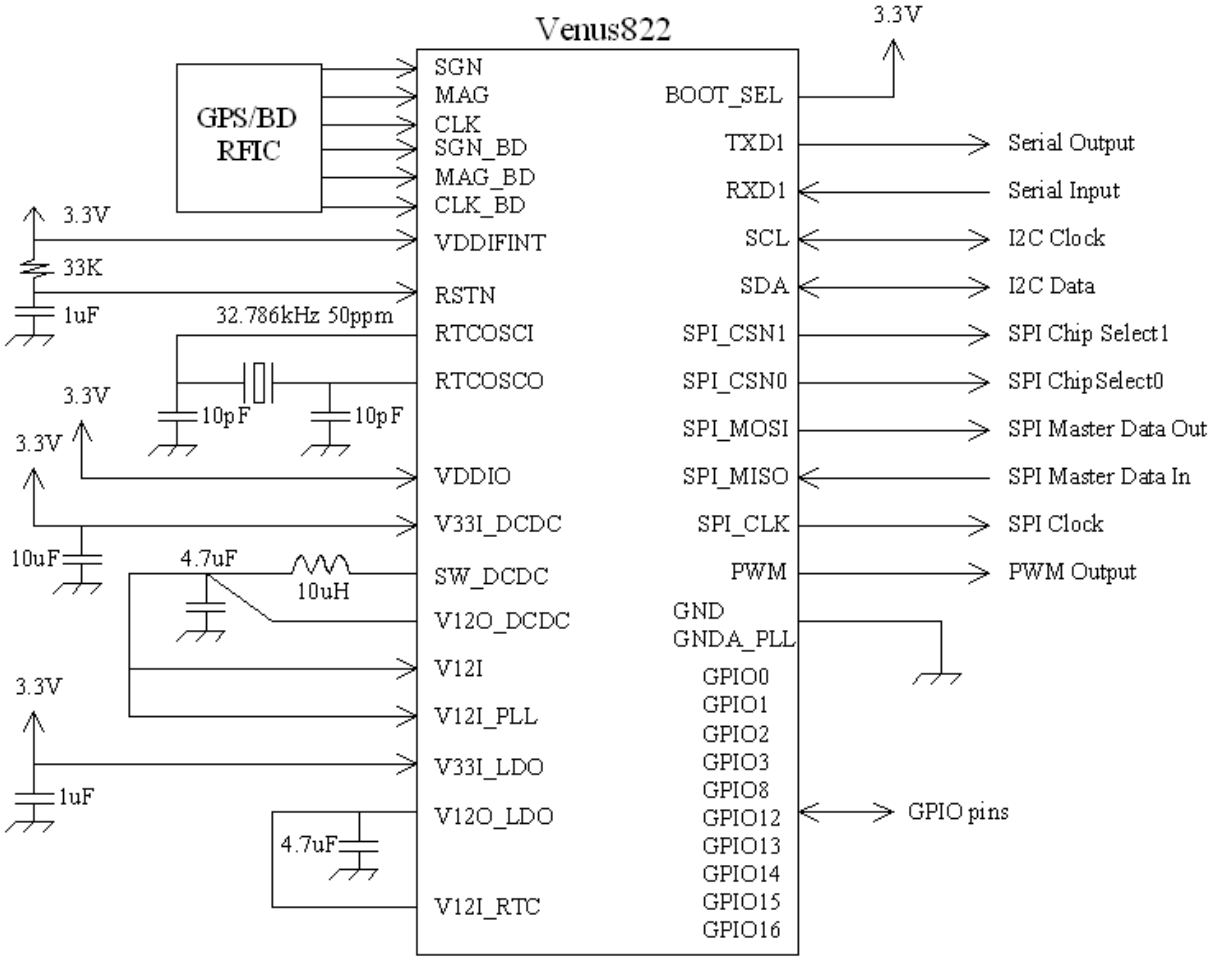


Figure-5 Minimal System for Venus822-BD

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Operating Temperature		-40	+85	^{o}C
Storage Temperature		-40	+150	^{o}C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Minimum	Typical	Maximum	Units
Core Supply Voltage	V12I	1.08	1.2	1.32	Volt
RTC Supply Voltage	V12I_RTC	1.08	1.2	1.32	Volt
PLL Supply Voltage	V12I_PLL	1.08	1.2	1.32	Volt
Supply Voltage for I/O Interface at 3.3V	VDDIO, VDDIFINT	2.97	3.3	3.63	Volt
Supply Voltage for I/O Interface at 1.8V	VDDIFINT	1.62	1.8	1.98	Volt
Junction Operating Temperature	Tj	-40	25	125	^{o}C

DC CHARACTERISTICS OF I/O INTERFACE AT 3.3V

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Condition**	**Units**
Input Low Voltage	V_{IL}	-0.3		0.8	LVTTL	Volt
Input High Voltage	V_{IH}	2.0		VDDIO+0.3 VDDIFINT+0.3	LVTTL	Volt
Output Low Voltage, Iol = 4mA	V_{OL}			0.4		Volt
Output High Voltage, Ioh = 4mA	V_{OH}	2.4				Volt
Input Pull-Up Resistance	R_{PU}	33	41	62		K-Ohm
Input Pull-Down Resistance	R_{PD}	33	42	68		K-Ohm
Input Leakage Current	I_{IN}			+/-10		uA

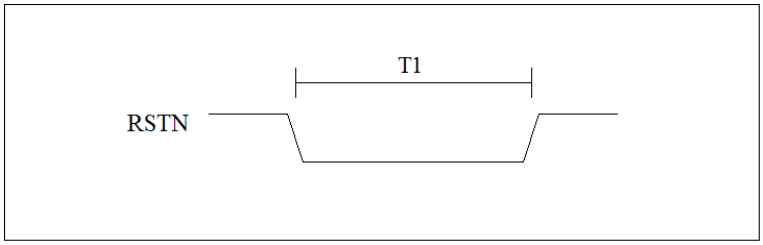
DC CHARACTERISTICS OF I/O INTERFACE AT 1.8V

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Condition**	**Units**
Input Low Voltage	V_{IL}	-0.3		0.35*VDDIO 0.35*VDDIFINT	LVTTL	Volt
Input High Voltage	V_{IH}	0.55*VDDIO 0.55*VDDIFINT		VDDIO+0.3 VDDIFINT+0.3	LVTTL	Volt
Output Low Voltage, Iol = 4mA	V_{OL}			0.45		Volt
Output High Voltage, Ioh = 4mA	V_{OH}	VDDIO-0.45 VDDIFINT-0.45				Volt
Input Pull-Up Resistance	R_{PU}	67	93	152		K-Ohm
Input Pull-Down Resistance	R_{PD}	64	92	170		K-Ohm
Input Leakage Current	I_{IN}			+/-10		uA

AC CHARACTERISTICS

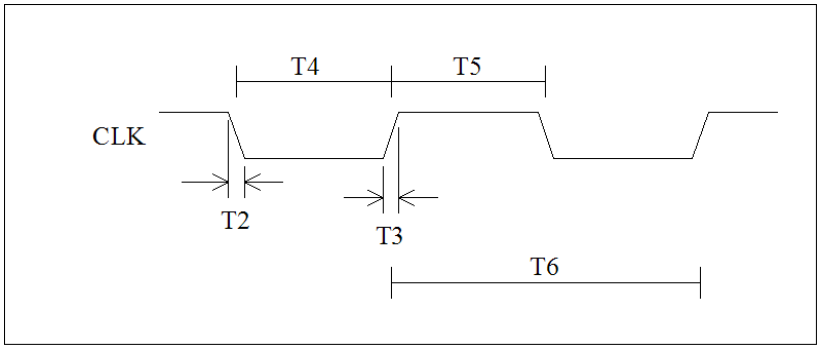
Reset Timing

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Reset duration	T1	10			CLK

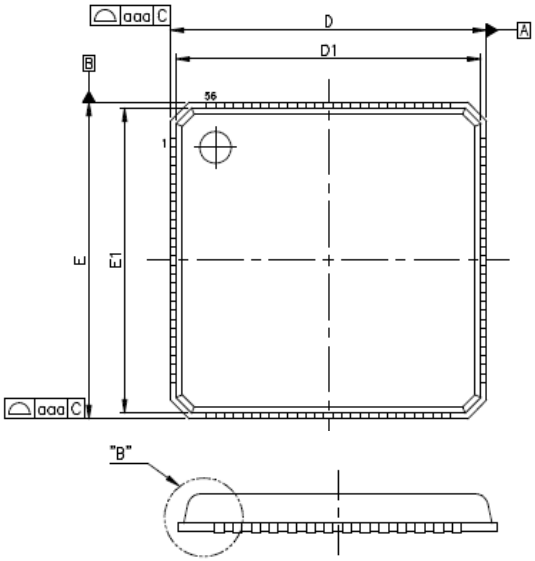


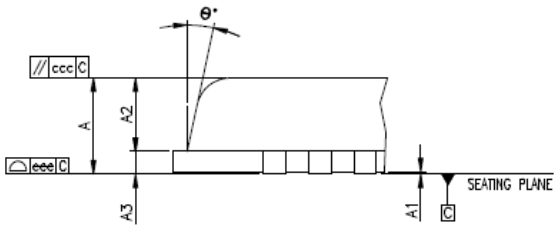
CLK Timing

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Fall Time	T2		4.5		ns
Rise Time	T3		4.5		ns
Clock Pulse Width Low	T4	12			ns
Clock Pulse Width High	T5	12			ns
Clock Period	T6	25			ns

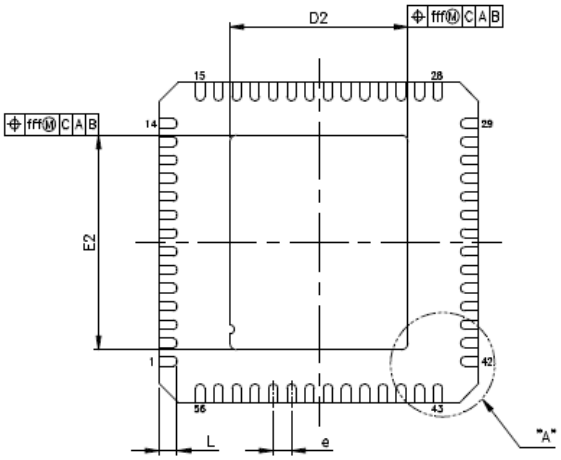


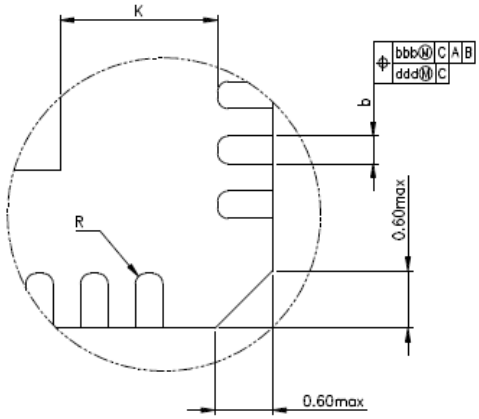
MECHANICAL SPECIFICATIONS





DETAIL "B"





DETAIL "A"

SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.203 REF.	
b	0.15	0.20	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D1	6.65	6.75	6.85
E1	6.65	6.75	6.85
e		0.40 BSC	
L	0.30	0.40	0.50
θ°	0	—	12
R	0.075	—	—
K	0.20	—	—
aaa	—	—	0.10
bbb	—	—	0.07
ccc	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08
fff	—	—	0.10

UNIT : mm

		D2			E2	
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
161X193MIL	3.75	3.90	4.05	4.55	4.70	4.85
⚠1 213X213MIL	5.00	5.20	5.40	5.00	5.20	5.40

UNIT : mm

NOTES :
1. JEDEC : MO-220 REV.K(VKKE)
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION "b" APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. THE PIN #1 IDENTIFIER EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. DIMENSION "A1" APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

MARKING INFORMATION

1320: date code

GK: internal code

RECOMMANDED REFLOW PROFILE FOR LEAD-FREE SOLDER PASTE

Follow: IPC/JEDEC J-STD-020 C

Condition:

Average ramp-up rate (217℃ to peak): 1~2℃/sec max.

Preheat：150~200C、60~180 seconds

Temperature maintained above 217℃ ：60~150 seconds

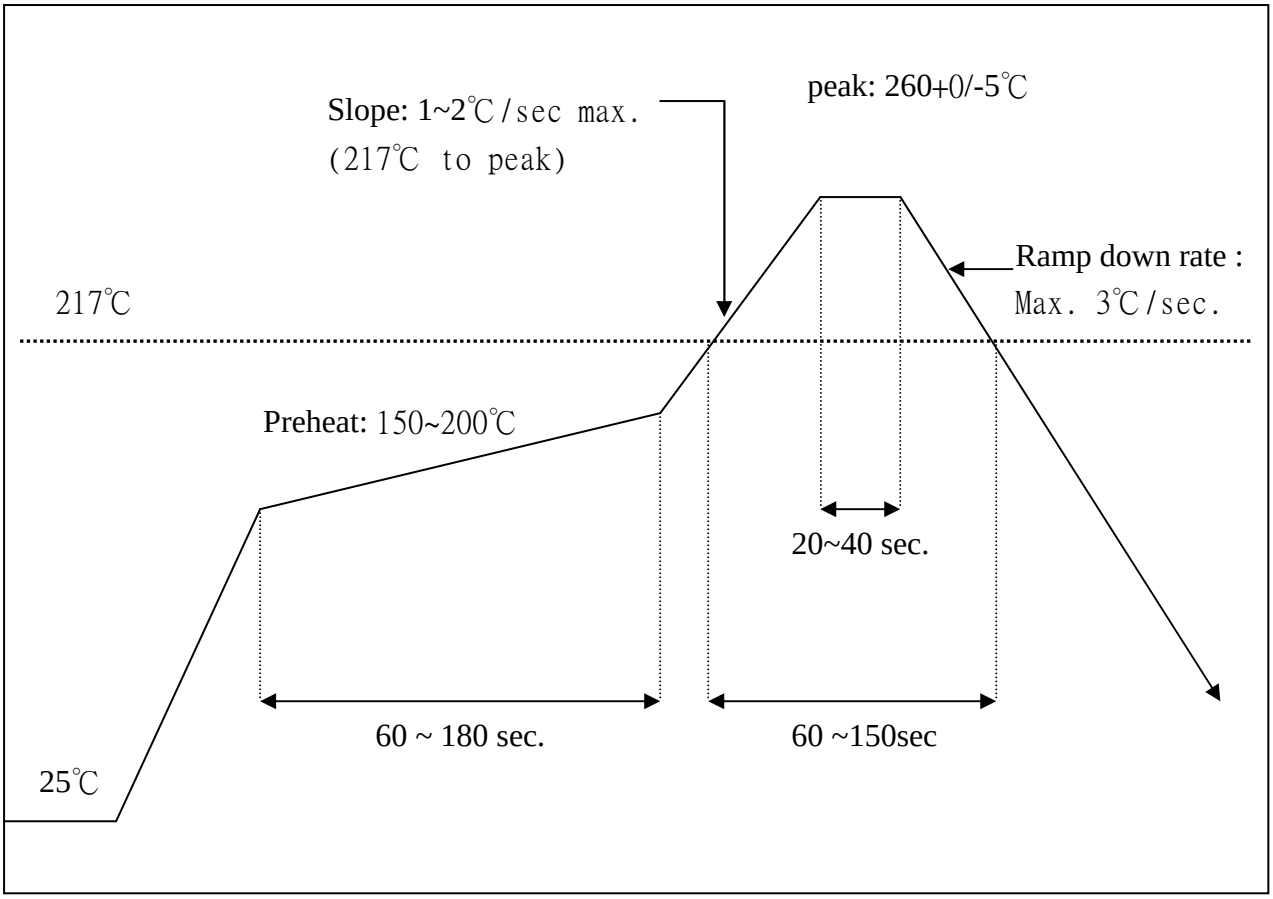
Time within 5℃ of actual peak temperature: 20 ~ 40 sec.

Peak temperature：260+0/-5℃

Ramp-down rate : 3℃/sec. max.

Time 25℃ to peak temperature : 8 minutes max.

Cycle interval：5 minutes



ORDERING INFORMATION

Part Number	Description
Venus822-BD	GPS/BD Baseband, 56 pin, QFN, Flash version

SkyTraq Technology, Inc.
4F, No.26, Minsiang Street, Hsinchu, Taiwan, 300
Phone: +886 3 5678650
Fax: +886 3 5678680
Email: info@skytraq.com.tw